National Semiconductor

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ADC12D040
Dual 12-Bit, 40 MSPS, 600 mW A/D Converter with Internal/External Reference

General Description

The ADC12D040 is a dual, low power monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 40 Megasamples per second (Msps), minimum. This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance. Operating on a single 5V power supply, the ADC12D040 achieves 10.9 effective bits at 10 MHz input and consumes just 600 mW at 40 Msps, including the reference current. The Power Down feature reduces power consumption to 75 mW.

The differential inputs provide a full scale differential input swing equal to $2V_{REF}$ with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. The digital outputs for the two ADCs are available on separate 12-bit buses with an output data format choice of offset binary or 2's complement.

For ease of interface, the digital output driver power pins of the ADC12D040 can be connected to a separate supply voltage in the range of 2.4V to the digital supply voltage, making the outputs compatible with low voltage systems. The ADC12D040's speed, resolution and single supply operation make it well suited for a variety of applications.

This device is available in the 64-lead TQFP package and will operate over the industrial temperature range of –40˚C to +85˚C. An evaluation board is available to facilitate the product evaluation process

Features

- Binary or 2's complement output format
- Single supply operation
- Internal sample-and-hold
- Outputs 2.4V to 5V compatible
- Power down mode
- Pin-compatible with ADC12DL066
- Internal/External Reference

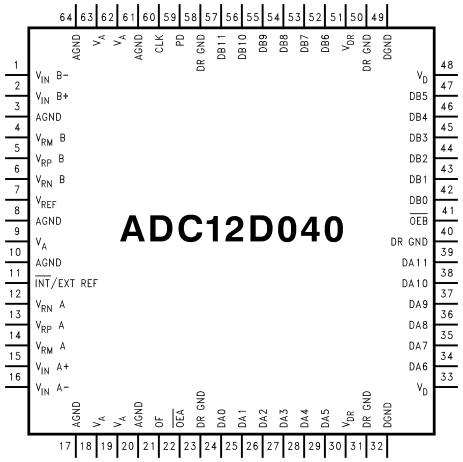
Key Specifications

■ SNR (f_{IN} = 10 MHz)	68 dB (typ)
■ ENOB (f_{IN} = 10 MHz)	10.9 bits (typ)
■ SFDR (f_{IN} = 10 MHz)	80 dB (typ)
■ Data Latency	6 Clock Cycles
■ Supply Voltage	+5V ±5%
■ Power Consumption, Operating	
— Operating	600 mW (typ)
— Power Down Mode	75 mW (typ)

Applications

- Ultrasound and Imaging
- Instrumentation
- Communications Receivers
- Sonar/Radar
- xDSL
- Cable Modems

Connection Diagram



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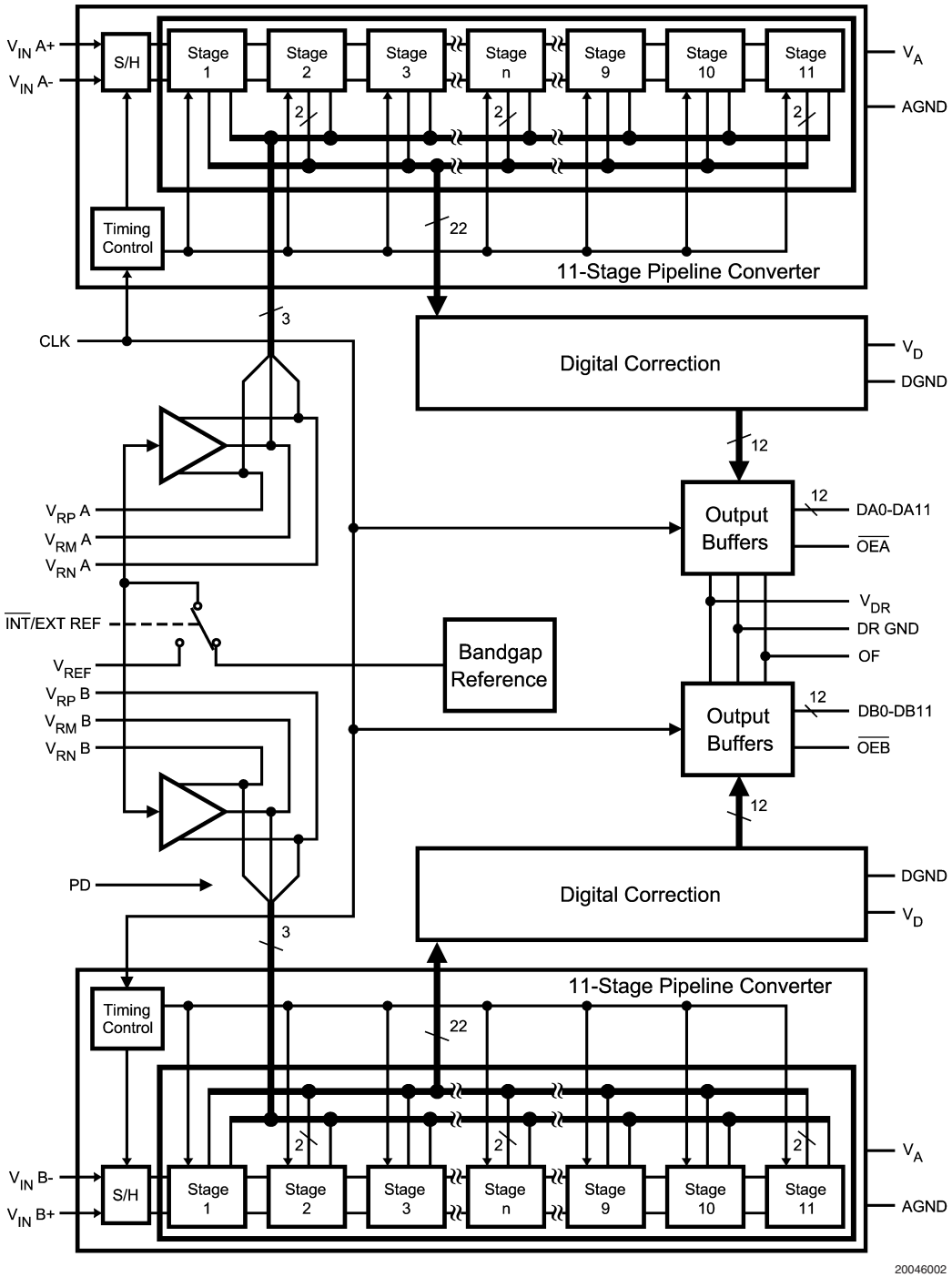
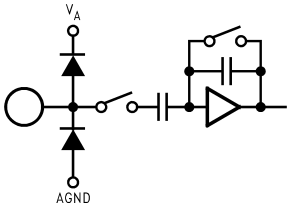
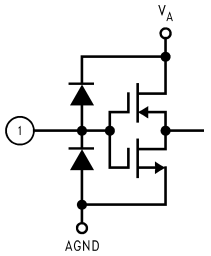
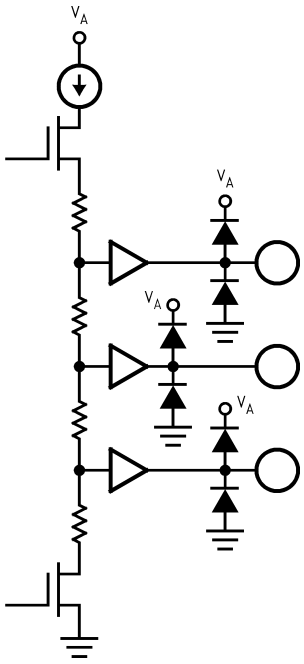
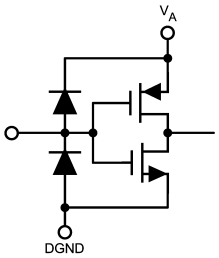
Ordering Information

Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC12D040CIVS	64 Pin TQFP
ADC12D040CIVSX	64 Pin TQFP Tape and Reel
ADC12D040EVAL	Evaluation Board

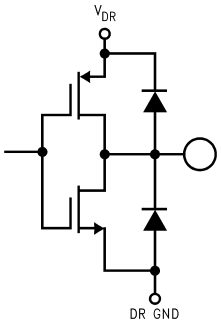
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
15 2	$V_{IN}A+$ $V_{IN}B+$		Non-Inverting analog signal Inputs. With a 2.0V reference the full-scale input signal level is 2.0 V_{P-P} on each pin of the input pair, centered on a common V_{CM}.
16 1	$V_{IN}A-$ $V_{IN}B-$		Inverting analog signal Input. With a 2.0V reference the full-scale input signal level is 2.0 V_{P-P} on each pin of the input pair, centered on a common V_{CM}. These (-) input pins may be connected to a common V_{CM} for single-ended operation, but a differential input signal is required for best performance.
7	V_{REF}		Reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor when external reference is used. V_{REF} is 2.0V nominal and should be between 1.0V to 2.4V.
11	$\overline{INT}$/EXT REF		V_{REF} select pin. With a logic low at this pin the internal 2.0V reference is selected. With a logic high on this pin an external reference voltage must be applied to V_{REF} input pin 7.
13 5	$V_{RP}A$ $V_{RP}B$		These pins are high impedance reference bypass pins only. Connect a 0.1 µF capacitor from each of these pins to AGND. DO NOT LOAD these pins.
14 4	$V_{RM}A$ $V_{RM}B$		
12 6	$V_{RN}A$ $V_{RN}B$		
DIGITAL I/O			
60	CLK		Digital clock input. The range of frequencies for this input is 100 kHz to 55 MHz (typical) with guaranteed performance at 40 MHz. The input is sampled on the rising edge of this input.
22 41	$\overline{OEA}$ $\overline{OEB}$		$\overline{OEA}$ and $\overline{OEB}$ are the output enable pins that, when low, enables their respective TRI-STATE® data output pins. When either of these pins is high, the corresponding outputs are in a high impedance state.
59	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.
21	OF		Output Format pin. A logic low on this pin causes output data to be in offset binary format. A logic high on this pin causes the output data to be in 2's complement format.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
24–29 34–39	DA0–DA11		Digital data output pins that make up the 12-bit conversion results of their respective converters. DA0 and DB0 are the LSBs, while DA11 and DB11 are the MSBs of the output word. Output levels are TTL/CMOS compatible.
42–47 52–57	DB0–DB11		
ANALOG POWER			
9, 18, 19, 62, 63	V_A		Positive analog supply pins. These pins should be connected to a quiet +5V source and bypassed to AGND with 0.1 µF monolithic capacitors located within 1 cm of these power pins, and with a 10 µF capacitor.
3, 8, 10, 17, 20, 61, 64	AGND		The ground return for the analog supply.
DIGITAL POWER			
33, 48	V_D		Positive digital supply pin. This pin should be connected to the same quiet +5V source as is V_A and be bypassed to DGND with a 0.1 µF monolithic capacitor located within 1 cm of the power pin and with a 10 µF capacitor.
32, 49	DGND		The ground return for the digital supply.
30, 51	V_{DR}		Positive digital supply pins for the ADC12D040's output drivers. These pins should be connected to a voltage source of +2.4V to +5V and bypassed to DR GND with a 0.1 µF monolithic capacitor. If the supply for these pins are different from the supply used for V_A and V_D, they should also be bypassed with a 10 µF tantalum capacitor. V_{DR} should never exceed the voltage on V_D. All bypass capacitors should be located within 1 cm of the supply pin.
23, 31, 40, 50, 58	DR GND		The ground return for the digital supply for the ADC12D040's output drivers. These pins should be connected to the system digital ground, but not be connected in close proximity to the ADC12D040's DGND or AGND pins. See Section 5 (Layout and Grounding) for more details.

Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_A, V_D, V_{DR}	6.5V
V_{DR}	V_D + 0.3V
$\|V_A - V_D\|$	≤ 100 mV
Voltage on Any Input or Output Pin	−0.3V to (V_A or V_D +0.3V)
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±50 mA
Package Dissipation at T_A = 25˚C	See (Note 4)
ESD Susceptibility	
Human Body Model (Note 5)	2500V
Machine Model (Note 5)	250V
Soldering Temperature, Infrared, 10 sec. (Note 6)	235˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature	−40˚C ≤ T_A ≤ +85˚C
Supply Voltage (V_A, V_D)	+4.75V to +5.25V
Output Driver Supply (V_{DR})	+2.35V to V_D
V_{REF} Input	1.0V to 2.4V
CLK, PD, $\overline{OE}$	−0.5V to (V_D + 0.5V)
Analog Input Pins	−0V to (V_A − 0.5V)
Input Common Mode Voltage (V_{CM})	V_{REF}/2 to V_A − V_{REF}
|AGND−DGND|	≤100mV

Package Thermal Resistance

Package	θ_{J-A}
64-Lead TQFP	50˚C / W

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A V_D +5V, V_{DR} +3.0V, PD = 0V, $\overline{INT}$/EXT = V_D, V_{REF} = +2.0V, $\overline{OEA}$, $\overline{OEB}$ = 0V, f_{CLK} = 40 MHz, t_r = t_f = 3 ns, C_L = 20 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25˚C (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**12**	Bits (min)
INL	Integral Non Linearity (Note 11)		±0.7	**±2.0**	LSB (max)
DNL	Differential Non Linearity		±0.4	**±1.0**	LSB (max)
GE	Gain Error	Positive Error	0.51	**+2.8/−1.9**	%FS
		Negative Error	0.68	**+4/−2.7**	%FS
TC GE	Gain Error Tempco	External Reference	15		ppm/ºC
		Internal Reference	100		ppm/ºC
V_{OFF}	Offset Error (V_{IN}+ = V_{IN}−)		−0.1	**±1.2**	%FS (max)
TC V_{OFF}	Offset Error Tempco	External Reference	3		ppm/ºC
		Internal Reference	3		ppm/ºC
	Under Range Output Code		0	**0**	
	Over Range Output Code		4095	**4095**	
DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth	0 dBFS Input, Output at −3 dB	100		MHz
SNR	Signal-to-Noise Ratio	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	69		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	68	**66.5**	dB (min)
SINAD	Signal-to-Noise and Distortion	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	69		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	68	**65.6**	dB (min)
ENOB	Effective Number of Bits	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	11.1		Bits
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	10.9	**10.6**	Bits (min)
THD	Total Harmonic Distortion	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	−80		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	−78	**−69**	dB (max)
H2	Second Harmonic	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS	−84		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS	−80	**−73**	dB (max)

Converter Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A V_D +5V, V_{DR} +3.0V, PD = 0V, $\overline{INT}$/EXT = V_D, V_{REF} = +2.0V, $\overline{OEA}$, $\overline{OEB}$ = 0V, f_{CLK} = 40 MHz, t_r = t_f = 3 ns, C_L = 20 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25˚C (Notes 7, 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 10)	Units (Limits)
H3	Third Harmonic	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS		−84		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS		−82	**−69.5**	dB (max)
SFDR	Spurious Free Dynamic Range	f_{IN} = 1 MHz, V_{IN} = −0.5 dBFS		84		dB
		f_{IN} = 10 MHz, V_{IN} = −0.5 dBFS		80	**69.5**	dB (min)
IMD	Intermodulation Distortion	f_{IN} = 9.6 MHz and 10.2 MHz, each = −6.0 dBFS		−80		dBFS
INTER-CHANNEL CHARACTERISTICS						
	Channel—Channel Offset Match			±0.02		%FS
	Channel—Channel Gain Error Match			±0.05		%FS
	Crosstalk	10 MHz Tested Channel. 15 MHz Other Channel		−80		dB
REFERENCE AND ANALOG INPUT CHARACTERISTICS						
C_{IN}	V_{IN} Input Capacitance (each pin to GND)	V_{IN} = 2.5 Vdc + 0.7 V_{rms}	(CLK LOW)	8		pF
			(CLK HIGH)	7		pF
V_{REF}	Input Reference Voltage (Note 13)			2.00	1.0	V (min)
					2.4	V (max)
R_{REF}	Reference Input Resistance			100		MΩ (min)
V_{IN}	Analog Input Voltage Range				0	V (min)
					4	V (max)

DC and Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +5V, V_{DR} = +3.0V, PD = 0V, $\overline{INT}$/EXT = V_D, V_{REF} = +2.0V, $\overline{OEA}$, $\overline{OEB}$ = 0V, f_{CLK} = 40 MHz, t_r = t_f = 3 ns, C_L = 20 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25˚C (Notes 7, 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 10)	Units (Limits)
CLK, PD, $\overline{OE}$ DIGITAL INPUT CHARACTERISTICS						
$V_{IN(1)}$	Logical “1” Input Voltage	V_D = 5.25V			**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_D = 4.75V			**1.0**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 5.0V		10		µA
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V		−10		µA
C_{IN}	Digital Input Capacitance			5		pF
D0–D11 DIGITAL OUTPUT CHARACTERISTICS						
$V_{OUT(1)}$	Logical “1” Output Voltage	I_{OUT} = −0.5 mA	V_{DR} = 2.5V		**2.3**	V (min)
			V_{DR} = 3V		**2.7**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = 1.6 mA, V_{DR} = 3V			**0.4**	V (max)
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 2.5V or 5V		100		nA
		V_{OUT} = 0V		−100		nA
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V		−20		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V_{DR}		20		mA
C_{OUT}	Digital Output Capacitance			5		pF

DC and Logic Electrical Characteristics (Continued)

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +5V, V_{DR} = +3.0V, PD = 0V, $\overline{INT}$/EXT = V_D, V_{REF} = +2.0V, $\overline{OEA}$, $\overline{OEB}$ = 0V, f_{CLK} = 40 MHz, t_r = t_f = 3 ns, C_L = 20 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25˚C (Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	PD Pin = DGND, V_{REF} = 2.0V PD Pin = V_{DR}	93 15	**110**	mA (max) mA
I_D	Digital Supply Current	PD Pin = DGND PD Pin = V_{DR}	16 0	**18**	mA (max) mA
I_{DR}	Digital Output Supply Current	PD Pin = DGND, C_L = 0 pF (Note 14) PD Pin = V_{DR}	10.5 0	**12**	mA (max) mA
	Total Power Consumption	PD Pin = DGND, C_L = 0 pF (Note 15) PD Pin = V_{DR}	600 75	**700**	mW mW
PSRR1	Power Supply Rejection	Rejection of Full-Scale Error with V_A = 4.75V vs. 5.25V	56		dB

AC Electrical Characteristics

Unless otherwise specified, the following specifications apply for AGND = DGND = DR GND = 0V, V_A = V_D = +5V, V_{DR} = +3.0V, PD = 0V, $\overline{INT}$/EXT = V_D, V_{REF} = +2.0V, $\overline{OEA}$, $\overline{OEB}$ = 0V, f_{CLK} = 40 MHz, t_r = t_f = 3 ns, C_L = 20 pF/pin. **Boldface limits apply for T_J = T_{MIN} to T_{MAX}:** all other limits T_J = 25˚C (Notes 7, 8, 9, 12)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 10)	Units (Limits)
f_{CLK}[1]	Maximum Clock Frequency			**40**	MHz (min)
f_{CLK}[2]	Minimum Clock Frequency		100		kHz
t_{CH}	Clock High Time		9		ns
t_{CL}	Clock Low Time		9		ns
t_{CONV}	Conversion Latency			**6**	Clock Cycles
t_{OD}	Data Output Delay after Rising CLK Edge	V_{DR} = 3.0V	10	**17.5**	ns (max)
t_{AD}	Aperture Delay		1.2		ns
t_{AJ}	Aperture Jitter		2		ps rms
t_{HOLD}	Clock Edge to Data Transition		8		ns
t_{DIS}	Data outputs into TRI-STATE Mode		4		ns
t_{EN}	Data Outputs Active after TRI-STATE		4		ns
t_{PD}	Power Down Mode Exit Cycle		500		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND DR GND = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND, or V_{IN} > V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

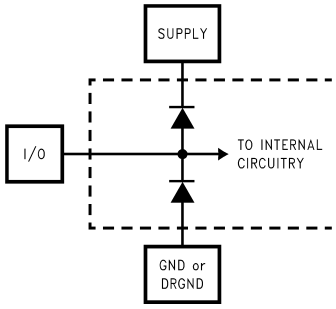
Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150˚C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature, (T_A), and can be calculated using the formula P_DMAX = ($T_J$max - T_A)/θ_{JA}. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.

Note 6: The 235˚C reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR), the following Conditions apply: Maintain the temperature at the top of the package body above 183˚C for a minimum 60 seconds. The temperature measured on the package body must not exceed 220˚C. Only one excursion above 183˚C is allowed per reflow cycle.

Note 7: The inputs are protected as shown below. Input voltage magnitudes above V_A or below GND will not damage this device, provided current is limited per (Note 3). However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 4.75V, the full-scale input voltage must be ≤4.85V to ensure accurate conversions.

AC Electrical Characteristics (Continued)



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Note 8: To guarantee accuracy, it is required that $|V_A - V_D| \leq 100$ mV and separate bypass capacitors are used at each power supply pin.

Note 9: With the test condition for V_{REF} = +2.0V ($4V_{P-P}$ differential input), the 12-bit LSB is 977 µV.

Note 10: Typical figures are at $T_A = T_J = 25^\circ C$, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive and negative full-scale.

Note 12: Timing specifications are tested at TTL logic levels, V_{IL} = 0.4V for a falling edge and V_{IH} = 2.4V for a rising edge.

Note 13: Optimum performance will be obtained by keeping the reference input in the 1.8V to 2.4V range. The LM4051CIM3-ADJ (SOT23 package) is recommended for this application.

Note 14: I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). $I_{DR}=V_{DR}(C_0 \times f_0 + C_1 \times f_1 + ...C_{11} \times f_{11})$ where V_{DR} is the output driver power supply voltage, C_n is total capacitance on the output pin, and f_n is the average frequency at which that pin is toggling.

Note 15: Excludes I_{DR}. See note 14.

Specification Definitions

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

CLOCK DUTY CYCLE is the ratio of the time during one cycle that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

COMMON MODE VOLTAGE (V_{CM}) is the d.c. potential present at both signal inputs to the ADC.

CONVERSION LATENCY See PIPELINE DELAY.

CROSSTALK is coupling of energy from one channel into the other channel.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Positive Full Scale Error – Negative Full-Scale Error

Gain Error can also be separated into Positive Gain Error and Negative Gain Error, which are.

PGE = Positive Full-Scale Error – Offset Error

NGE = Offset Error – Negative Full-Scale Error

GAIN ERROR MATCHING is the difference in gain errors between the two converters divided by the average gain of the converters.

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $V_{REF} / 2^n$, where "n" is the ADC resolution in bits, which is 12 in the case of the ADC12D040.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC12D040 is guaranteed not to have any missing codes.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL SCALE ERROR is the difference between the actual first code transition and its ideal value of ½ LSB above negative full scale.

OFFSET ERROR is the difference between the two input voltages ($V_{IN}+ - V_{IN}-$) required to cause a transition from code 2047 to 2048.

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

OVER RANGE RECOVERY TIME is the time required after V_{IN} goes from a specified voltage out of the normal input range to a specified voltage within the normal input range and the converter makes a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC12D040, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the d.c. power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected at the output.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB, of the rms total of the first seven harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

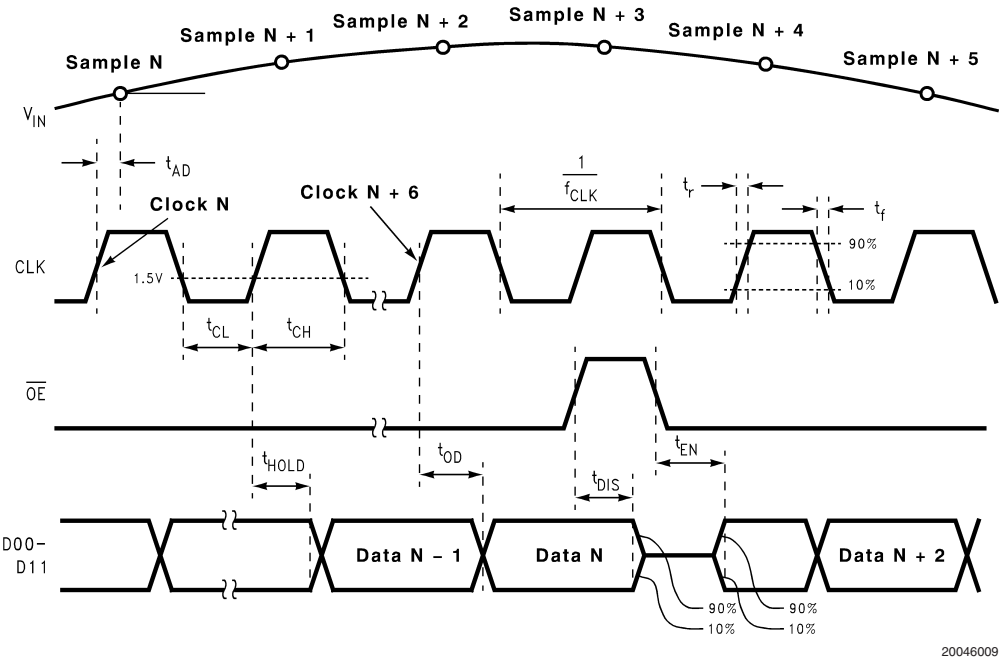
$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_{10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagram



Output Timing

Transfer Characteristic

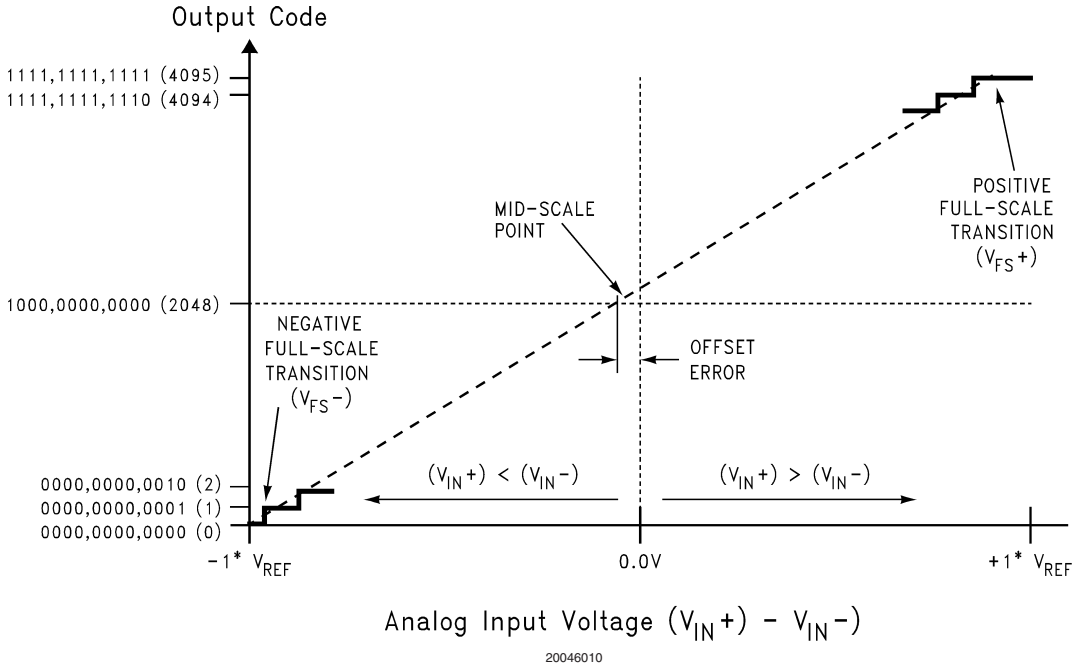
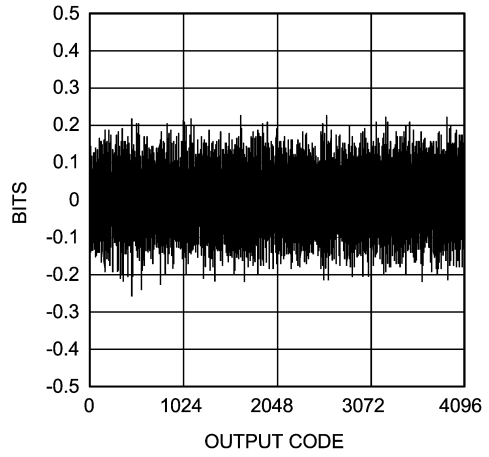


FIGURE 1. Transfer Characteristic

Typical Performance Characteristics

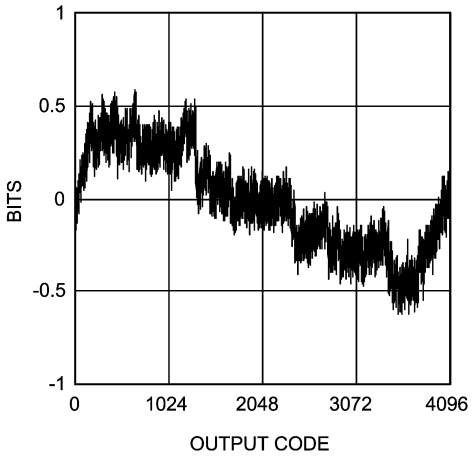
V_A = V_D = 5V, V_{DR} = 3V, f_{CLK} = 40 MHz, f_{IN} = 10 MHz unless otherwise stated

DNL



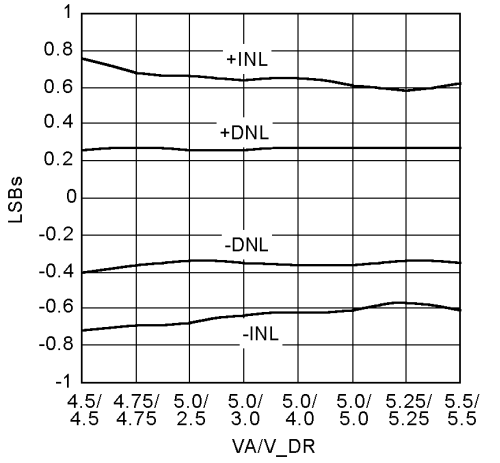
20046036

INL



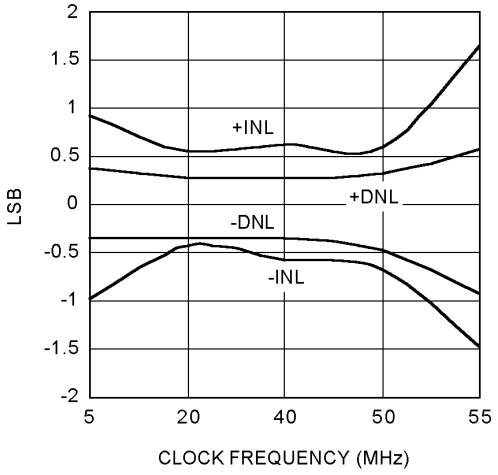
20046037

INL & DNL vs. Supply Voltage



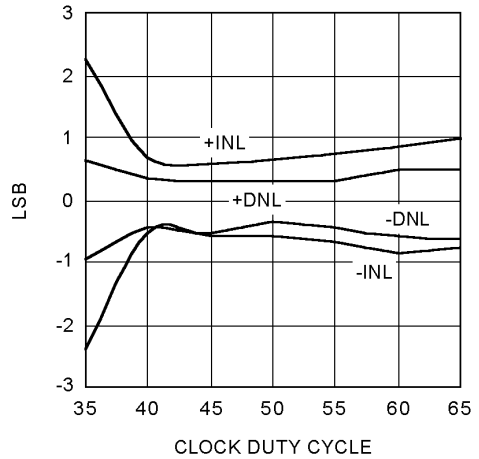
20046038

DNL & INL vs. Clock Frequency



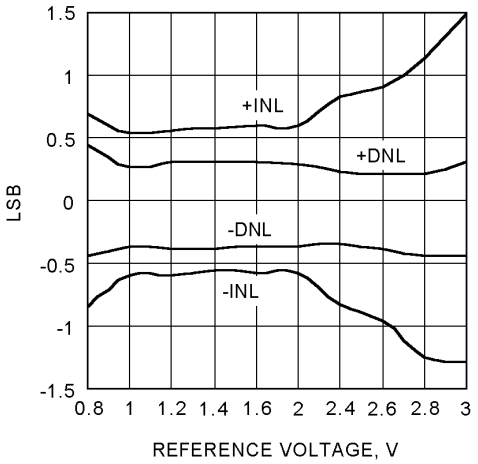
20046044

DNL & INL vs. Clock Duty Cycle



20046047

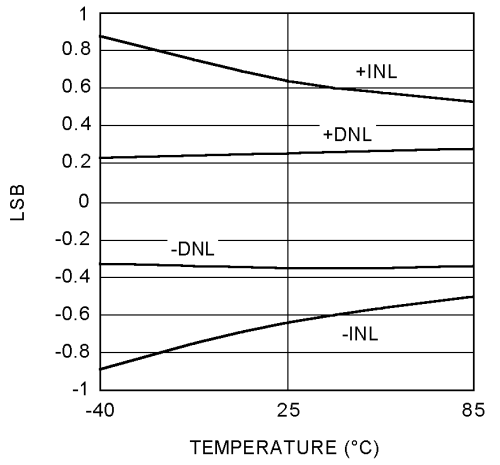
DNL & INL vs. Reference Voltage



20046050

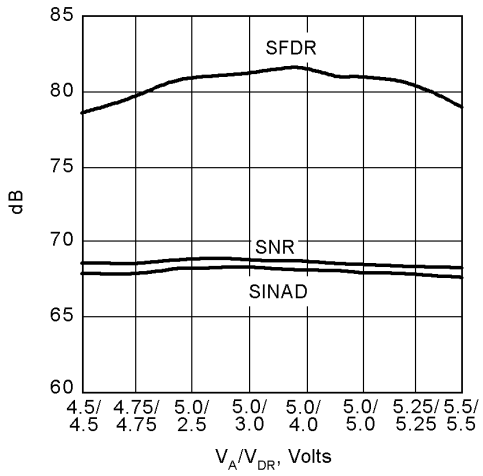
Typical Performance Characteristics $V_A = V_D = 5V$, $V_{DR} = 3V$, $f_{CLK} = 40$ MHz, $f_{IN} = 10$ MHz unless otherwise stated (Continued)

INL & DNL vs. Temperature



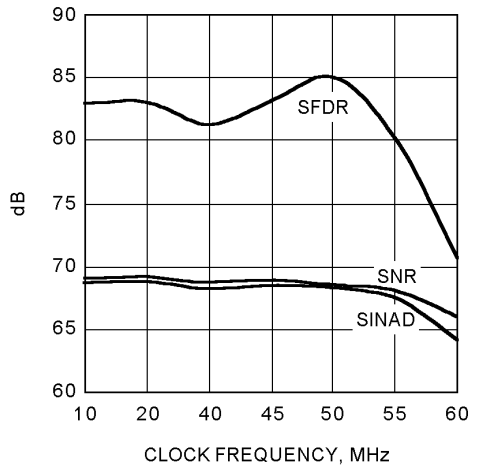
20046039

SNR, SINAD, SFDR vs. Supply Voltage



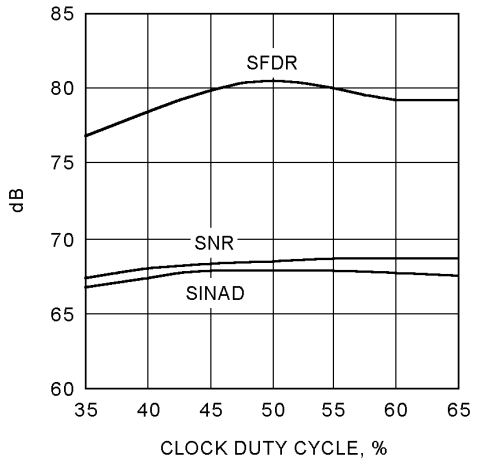
20046040

SNR, SINAD, SFDR vs. Clock Frequency



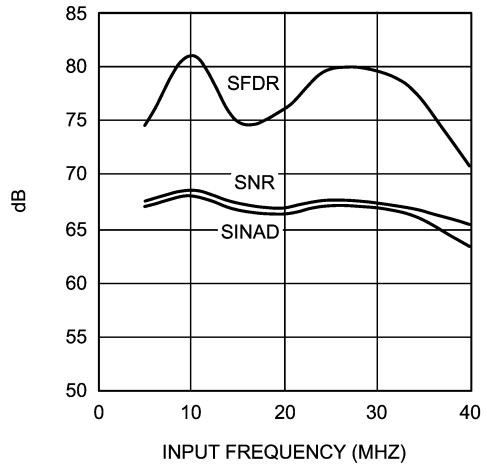
20046045

SNR, SINAD, SFDR vs. Clock Duty Cycle



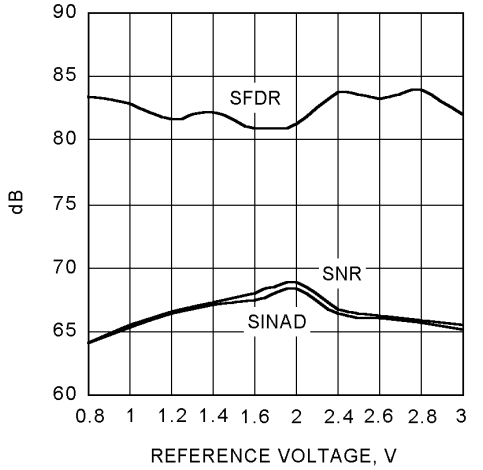
20046048

SNR, SINAD, SFDR vs. Input Frequency



20046042

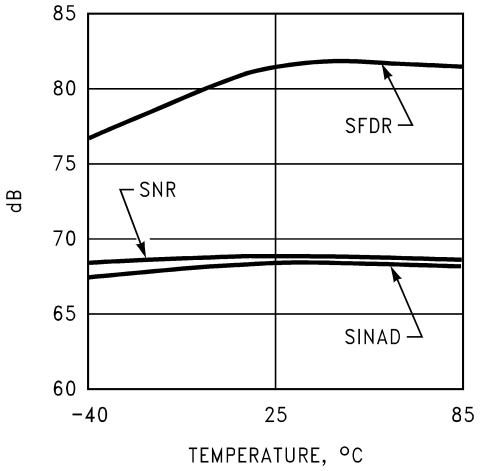
SNR, SINAD, SFDR vs. Reference Voltage



20046051

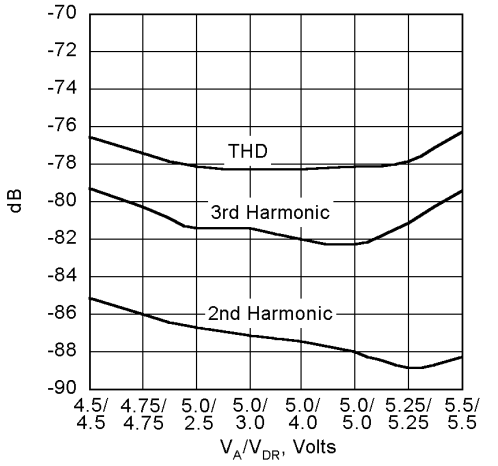
Typical Performance Characteristics $V_A = V_D = 5V$, $V_{DR} = 3V$, $f_{CLK} = 40$ MHz, $f_{IN} = 10$ MHz unless otherwise stated (Continued)

SNR, SINAD, SFDR vs. Temperature



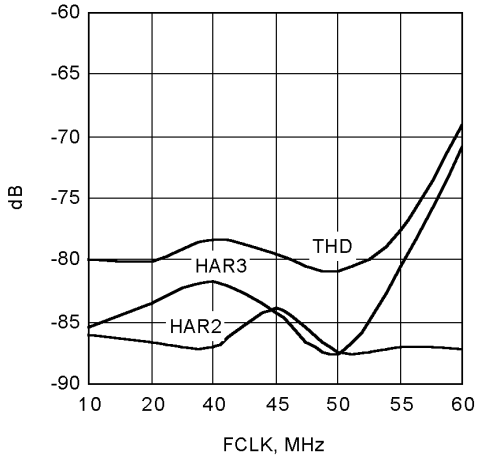
20046058

Distortion vs. Supply Voltage



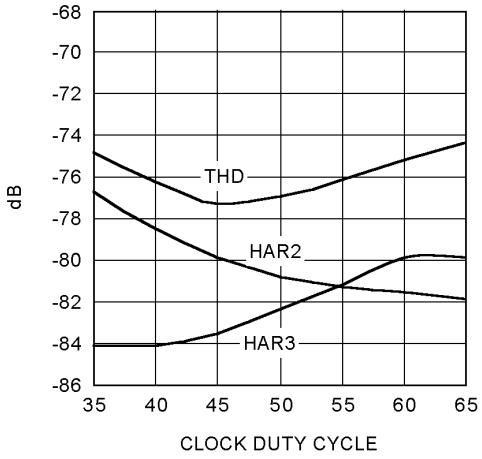
20046041

Distortion vs. Clock Frequency



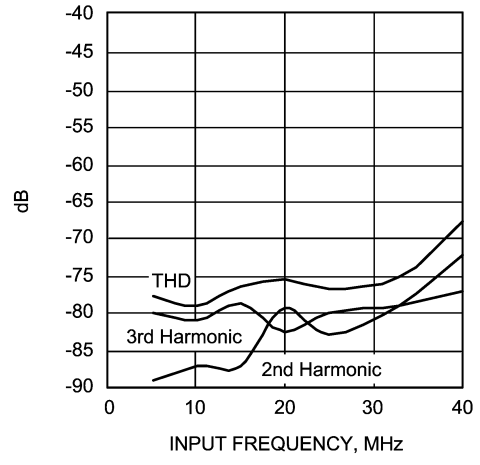
20046046

Distortion vs. Clock Duty Cycle



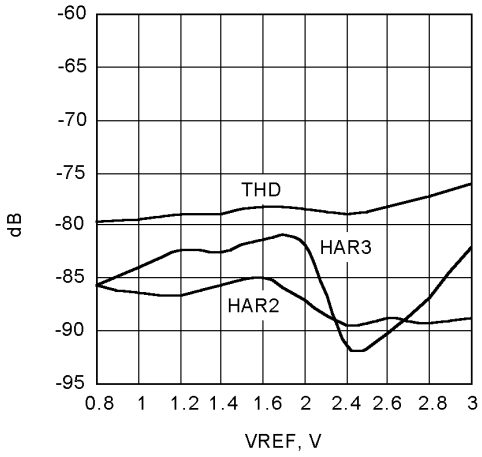
20046049

Distortion vs. Input Frequency



20046043

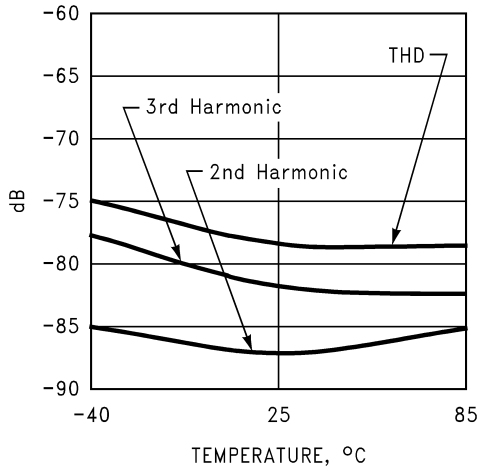
Distortion vs. Reference Voltage



20046052

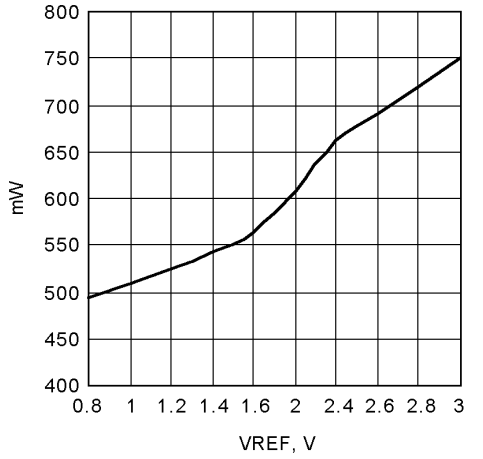
Typical Performance Characteristics $V_A = V_D = 5V$, $V_{DR} = 3V$, $f_{CLK} = 40$ MHz, $f_{IN} = 10$ MHz unless otherwise stated (Continued)

Distortion vs. Temperature



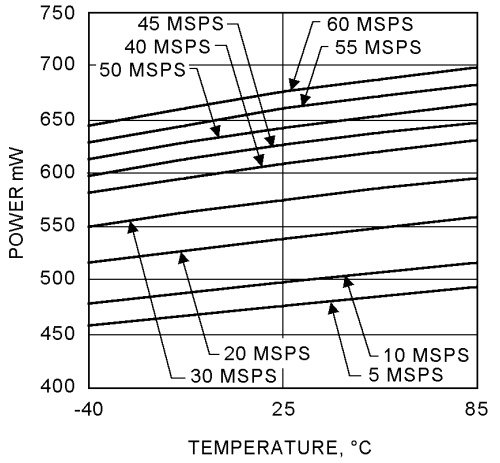
20046059

Power Consumption vs. Reference Voltage



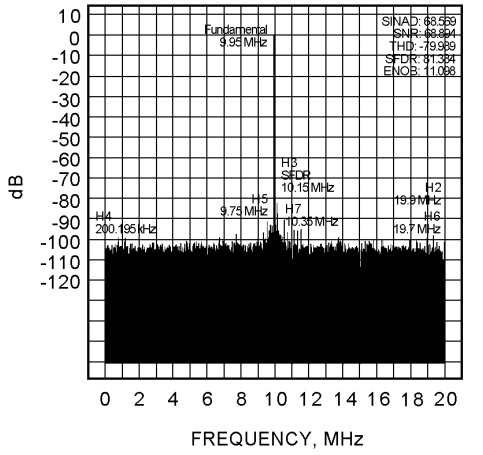
20046053

Power Consumption vs. Temperature



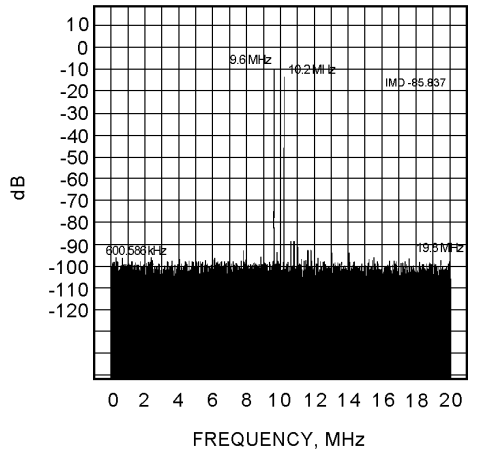
20046054

Spectral Response @ Fin = 9.95 MHz, F_{CLK} = 40 MHz



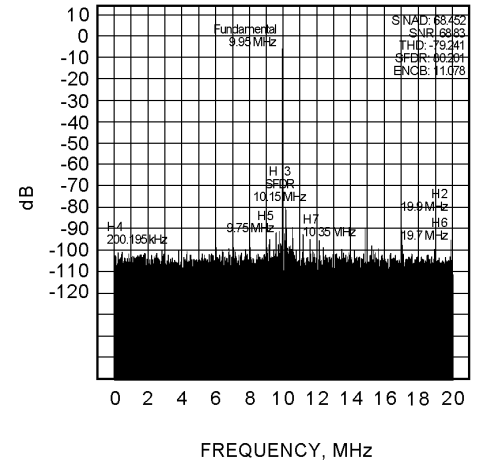
20046055

IMD Response Fin = 9.6 MHz, 10.2 MHz, F_{CLK} = 40 MHz



20046056

Crosstalk Response Fin = 9.95 MHz, $F_{CROSSTALK}$ = 15 MHz, F_{CLK} = 40 MHz



20046057

Functional Description

Operating on a single +5V supply, the ADC12D040 uses a pipeline architecture and has error correction circuitry to help ensure maximum performance. The differential analog input signal is digitized to 12 bits and the reference input is buffered to ease the task of driving that pin.

The output word rate is the same as the clock frequency, which can be between 100 ksps (typical) and 40 Msps with fully specified performance at 40 Msps. The analog input voltage for both channels is acquired at the rising edge of the clock and the digital data for a given sample is delayed by the pipeline for 6 clock cycles. A choice of Offset Binary or Two's Complement output format is selected with the OF pin.

A logic high on the power down (PD) pin reduces the converter power consumption to 75 mW.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12D040:

$4.75V \le V_A \le 5.25V$

$V_D = V_A$

$2.35V \le V_{DR} \le V_D$

$V_{REF}/2 \le V_{CM} \le V_A - V_{REF}$

$100\ kHz \le f_{CLK} \le 40\ MHz$

$1.0V \le V_{REF} \le 2.4V$

1.1 Analog Inputs

The ADC12D040 has two analog signal inputs, $V_{IN}+$ and $V_{IN}-$. These two pins form a differential input pair. There is one reference input pin, V_{REF}.

The analog input circuitry contains an input boost circuit that provides improved linearity over a wide range of analog input voltages. To prevent an on-chip over voltage condition that could impair device reliability, the input signal should never exceed the voltage described as

$$V_A - V_{REF}/2.$$

1.2 Reference Pins

The ADC12D040 is designed to operate with a 2.0V reference, but performs well with reference voltages in the range of 1.0V to 2.4V. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC12D040. Increasing the reference voltage (and the input signal swing) beyond 2.4V may degrade THD for a full-scale input especially at higher input frequencies. It is important that all grounds associated with the reference voltage and the input signal make connection to the analog ground plane at a single point in that plane to minimize the effects of noise currents in the ground path.

The ADC12040 will perform well with reference voltages up to 2.4V for full-scale input frequencies up to 10 MHz. However, more headroom is needed as the input frequency increases, so the maximum reference voltage (and input swing) will decrease for higher full-scale input frequencies.

The six Reference Bypass Pins ($V_{RP}A$, $V_{RM}A$, $V_{RN}A$, $V_{RP}B$, $V_{RM}B$ and $V_{RN}B$) are made available for bypass purposes. These pins should each be bypassed to ground with a 0.1 µF capacitor. Smaller capacitor values will allow faster recovery from the power down mode, but may result in degraded noise performance. DO NOT LOAD these pins. Loading any of these pins may result in performance degradation.

The nominal voltages for the reference bypass pins are as follows:

$V_{RM}A = V_{RM}B = V_A / 2$

$V_{RP}A = V_{RP}B = V_{RM} + V_{REF} / 2$

$V_{RN}A = V_{RN}B = V_{RM} - V_{REF} / 2$

The V_{RN} pins may be used as a common mode voltage source (V_{CM}) for the analog input pins as long as no d.c. current is drawn from it. However, because the voltages at these pins are half that of the V_A supply pin, using these pins for a common mode source will result in reduced input headroom (the difference between the V_A supply voltage and the peak signal voltage at either analog input) and the possibility of reduced THD and SFDR performance. For this reason, it is recommended that V_A always exceed V_{REF} by at least 2 Volts. For high input frequencies it may be necessary to increase this headroom to maintain THD and SFDR performance.

1.3 Signal Inputs

The signal inputs are $V_{IN}+$ and $V_{IN}-$. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}+) - (V_{IN}-)$$

Figure 2 shows the expected input signal range.

Note that the common mode input voltage range is 1V to 3V with a nominal value of $V_A/2$. The input signals should remain between ground and 4V.

The Peaks of the individual input signals ($V_{IN}+$ and $V_{IN}-$) should each never exceed the voltage described as

$$V_{IN}+,\ V_{IN}- = (V_{REF} / 2 + V_{CM}) \le 4V \text{ (differential)}$$

to maintain THD and SINAD performance.

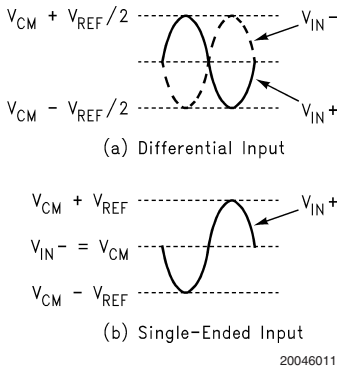


FIGURE 2. Expected Input Signal Range

The ADC12D040 performs best with a differential input with each input centered around a common V_{CM}. The peak-to-peak voltage swing at both $V_{IN}+$ and $V_{IN}-$ should not exceed the value of the reference voltage or the output data will be clipped.

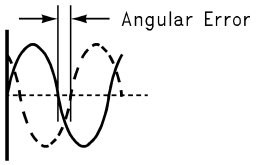
The two input signals should be exactly 180° out of phase from each other and of the same amplitude. For single frequency inputs, angular errors result in a reduction of the effective full scale input. For a complex waveform, however, angular errors will result in distortion.

For single frequency sine waves with angular errors of less than 45° (π/4) between the two inputs, the full scale error in LSB can be described as approximately

$$E_{FS} = 2^{(n-1)} * (1 - \cos (dev)) = 2048 * (1 - \cos (dev))$$

Applications Information (Continued)

Where dev is the angular difference between the two signals having a 180˚ relative phase relationship to each other (see *Figure 3*). Drive the analog inputs with a source impedance less than 100Ω.



20046012

FIGURE 3. Angular Errors Between the Two Input Signals Will Reduce the Output Level or Cause Distortion

TABLE 1. Input to Output Relationship – Differential Input

V_{IN}^+	V_{IN}^-	Binary Output	2's Complement Output
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	0000 0000 0000	1000 0000 0000
$V_{CM} - V_{REF/4}$	$V_{CM} + V_{REF}/4$	0100 0000 0000	1100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000	0000 0000 0000
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	1100 0000 0000	0100 0000 0000
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	1111 1111 1111	0111 1111 1111

TABLE 2. Input to Output Relationship – Single-Ended Input

V_{IN}^+	V_{IN}–	Binary Output	2's Complement Output
$V_{CM} - V_{REF}$	V_{CM}	0000 0000 0000	1000 0000 0000
$V_{CM} - V_{REF}/2$	V_{CM}	0100 0000 0000	1100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000	0000 0000 0000
$V_{CM} + V_{REF}/2$	V_{CM}	1100 0000 0000	0100 0000 0000
$V_{CM} + V_{REF}$	V_{CM}	1111 1111 1111	0111 1111 1111

1.3.1 Single-Ended Operation

Single-ended performance is lower than with differential input signals. For this reason, single-ended operation is not recommended. However, if single ended-operation is required and the resulting performance degradation is acceptable, one of the analog inputs should be connected to the d.c. mid point voltage of the driven input. The peak-to-peak differential input signal should be twice the reference voltage to maximize SNR and SINAD performance (*Figure 2*b).

For example, set V_{REF} to 1.0V, bias V_{IN}– to 2.5V and drive V_{IN}+ with a signal range of 1.5V to 3.5V.

Because very large input signal swings can degrade distortion performance, better performance with a single-ended input can be obtained by reducing the reference voltage when maintaining a full-range output. *Table 1* and *Table 2* indicate the input to output relationship of the ADC12D040.

1.3.2 Driving the Analog Input

The V_{IN}+ and the V_{IN}– inputs of the ADC12D040 consist of an analog switch followed by a switched-capacitor amplifier. The capacitance seen at the analog input pins changes with the clock level, appearing as 8 pF when the clock is low, and 7 pF when the clock is high.

As the internal sampling switch opens and closes, current pulses occur at the analog input pins, resulting in voltage spikes at the signal input pins. As a driving amplifier attempts to counteract these voltage spikes, a damped oscillation may appear at the ADC analog inputs. The best amplifiers for driving the ADC12D040 input pins must be able to react to these spikes and settle before the switch opens and another sample is taken. The LMH6702 LMH6628 and the LMH6622, LMH6655 are good amplifiers for driving the ADC12D040.

To help isolate the pulses at the ADC input from the amplifier output, use RCs at the inputs, as can be seen in *Figure 4* and *Figure 5*. These components should be placed close to the ADC inputs because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter that input.

For Nyquist applications the RC pole should be at the ADC sample rate. The ADC input capacitance in the sample mode should be considered when setting the RC pole. Setting the pole in this manner will provide best SNR performance.

To obtain best SINAD and ENOB performance, reduce the RC time constant until SNR and THD are numerically equal to each other. To obtain best distortion and SFDR performance, eliminate the RC altogether.

For undersampling applications, RC pole should be set at about 1.5 to 2 times the maximum input frequency to maintain a linear delay response.

Note that the ADC12DL040 is not designed to operate with single-ended inputs. However, doing so is possible if the degraded performance is acceptable. See Section 1.3.1.

Figure 4 shows a narrow band application with a transformer used to convert single-ended input signals to differential. *Figure 5* shows the use of a fully differential amplifier for single-ended to differential conversion.

Applications Information (Continued)

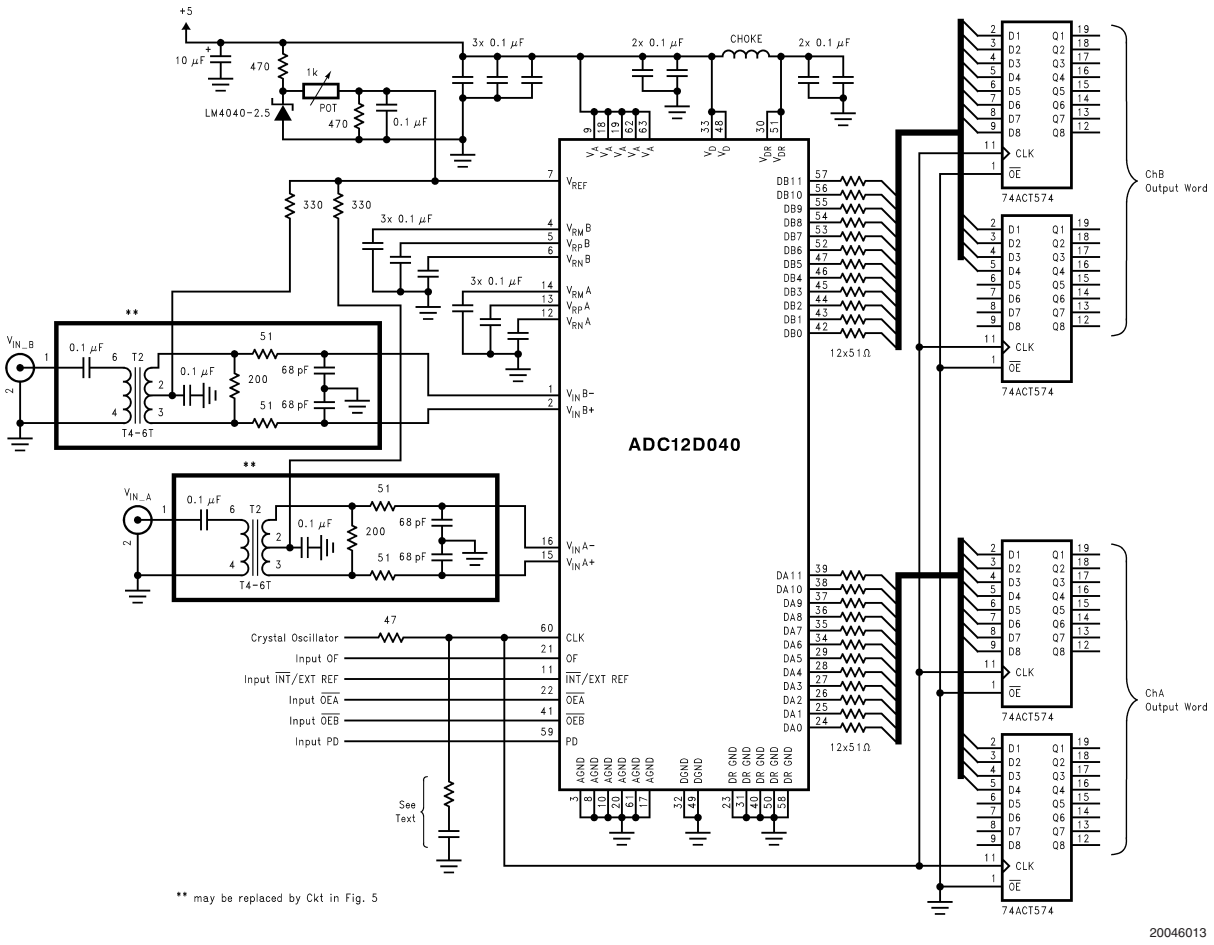


FIGURE 4. Application Circuit using Transformer or Differential Op-Amp Drive Circuit

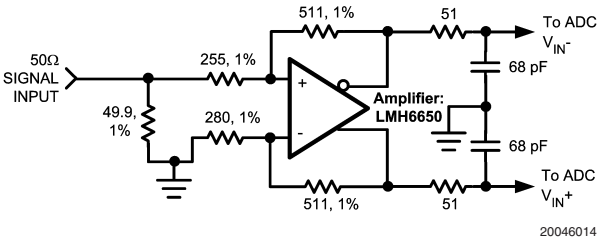


FIGURE 5. Differential Drive Circuit using a fully differential amplifier.

1.3.3 Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be of a value such that the peak excursions of the analog signal does not go more negative than ground or more positive than 1.0 Volts below the V_A supply voltage. The nominal V_{CM} should generally be about $V_{REF}/2$. $V_{RB}A$ and $V_{RB}B$ can be used as V_{CM} sources as long as no d.c. current is drawn from these pins.

2.0 DIGITAL INPUTS

Digital TTL/CMOS compatible inputs consist of CLK, $\overline{OEA}$, $\overline{OEB}$, OF, $\overline{INT}$/EXT REF, and PD.

2.1 CLK

The **CLK** signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the range of 100 kHz to 55 MHz with rise and fall times of less than 3ns. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90˚.

If the **CLK** is interrupted, or its frequency too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample

Applications Information (Continued)

The ADC clock line should be considered to be a transmission line and be series terminated at the source end to match the source impedance with the characteristic impedance of the clock line. It generally is not necessary to terminate the far (ADC) end of the clock line, but if a single clock source is driving more than one device (a condition that is generally not recommended), far end termination may be needed. Far end termination is a series RC with the resistor being the same as the characteristic impedance of the clock line. The capacitor should have a minimum value of

$$C \geq \frac{4 \times t_{PD} \times L}{Z_0}$$

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where t_{PD} is the propagation time in ns/unit length, "L" is the length of the line and Z_O is the characteristic impedance of the line. The units of t_{PD} and "L" should be consistent with each other. The typical board of FR-4 material has a t_{PD} of about 150 ps/inch, or about 60 ps/cm.

The far end termination should be near but beyond the ADC clock pin as seen from the clock source.

The duty cycle of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12040 is designed to maintain performance over a range of duty cycles. While it is specified and performance is guaranteed with a 50% clock duty cycle, performance is typically maintained over a clock duty cycle range of 40% to 60%.

Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 for information on setting characteristic impedance.

2.2 $\overline{\text{OEA}}$, $\overline{\text{OEB}}$

The $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ pin, when high, put the output pins of their respective converters into a high impedance state. When either of these pins is low the corresponding outputs are in the active state. The ADC12D040 will continue to convert whether these pins are high or low, but the output can not be read while the pin is high.

Since ADC noise increases with increased output capacitance at the digital output pins, do not use the TRI-STATE outputs of the ADC12L066 to drive a bus. Rather, each output pin should be located close to and drive a single digital input pin. To further reduce ADC noise, a 100 Ω resistor in series with each ADC digital output pin, located close to their respective pins, should be added to the circuit.

2.3 The PD Pin

The PD pin, when high, holds the ADC12D040 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 75 mW with a 40 MHz clock and 40mW if the clock is stopped when PD is high. The output data pins are undefined in the power down mode and the data in the pipeline is corrupted while in the power down mode.

The Power Down Mode Exit Cycle time is determined by the value of the capacitors on pins 4, 5, 6, 12, 13 and 14. These capacitors loose their charge in the Power Down mode and must be recharged by on-chip circuitry before conversions can be accurate. Smaller capacitor values allow faster recovery from the power down mode, but can result in a reduction in SNR, SINAD and ENOB performance.

2.4 The OF Pin

The output data format is offset binary when the OF pin is at a logic low or 2's complement when the OF pin is at a logic high. While the sense of this pin may be changed "on the fly," doing this is not recommended as the output data could be erroneous for a few clock cycles after this change is made.

2.5 The $\overline{\text{INT}}$/EXT REF Pin

The $\overline{\text{INT}}$/EXT REF pin determines whether the internal reference or an external reference voltage is used. With this pin at a logic low, the internal 2.0V reference is in use. With this pin at a logic high an external reference must be applied to the V_{REF} pin, which should then be bypassed to ground. There is no need to bypass the V_{REF} pin when the internal reference is used. There is no access to the internal reference voltage, but its value is approximately equal to $V_{RP} - V_{RN}$. See Section 1.2

3.0 DATA OUTPUT PINS

The ADC12D040 has 24 TTL/CMOS compatible Data Output pins. Valid data is present at these outputs while the $\overline{\text{OE}}$ and PD pins are low. While the t_{OD} time provides information about output timing, t_{OD} will change with a change of clock frequency. At the rated 40 MHz clock rate, the data transition is about 6 to 10 ns after the rise of the clock and about 4 to 10 ns before the fall of the clock (depending upon V_{DR}), so either clock edge may be used to capture data, depending upon the data setup time of the circuit accepting the data. Also, circuit board layout will affect relative delays of the clock and data, so it is important to consider these relative delays when designing the digital interface. At sample frequencies below 40 MHz, there is a longer time between data transition and the fall of the clock, so that the *falling edge* of the clock is generally the best edge to use for output data capture at low sample rates.

Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can cause on-chip ground noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 20 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance.

To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by connecting buffers (74AC541, for example) between the ADC outputs and any other circuitry. Only one driven input should be connected to each output pin. Additionally, inserting series resistors of about 100Ω at the digital outputs, close to the ADC pins, will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. See *Figure 4*.

Note that, although the ADC12D040 has Tri-State outputs, these outputs should not be used to drive a bus and the charging and discharging of large capacitances can degrade SNR performance. Each output pin should drive only one pin of a receiving device and the interconnecting lines should be as short as practical.

Applications Information (Continued)

4.0 POWER SUPPLY CONSIDERATIONS

The power supply pins should be bypassed with a 10 µF capacitor and with a 0.1 µF ceramic chip capacitor within a centimeter of each power pin. Leadless chip capacitors are preferred because they have low series inductance.

As is the case with all high-speed converters, the ADC12D040 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even on a transient basis. Be especially careful of this during turn on and turn off of power.

The V_{DR} pin provides power for the output drivers and may be operated from a supply in the range of 2.35V to V_D (nominal 5V). This can simplify interfacing to low voltage devices and systems. Note, however, that t_{OD} increases with reduced V_{DR}. **DO NOT operate the V_{DR} pin at a voltage higher than V_D.**

5.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Maintaining separate analog and digital areas of the board, with the ADC12D040 between these areas, is required to achieve specified performance.

The ground return for the data outputs (DR GND) carries the ground current for the output drivers. The output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DR GND pins should NOT be connected to system ground in close proximity to any of the ADC12D040's other ground pins.

Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry, and to keep the clock line as short as possible.

The effects of the noise generated from the ADC output switching can be minimized through the use of 100Ω resistors in series with each data output line. Locate these resistors as close to the ADC output pins as possible.

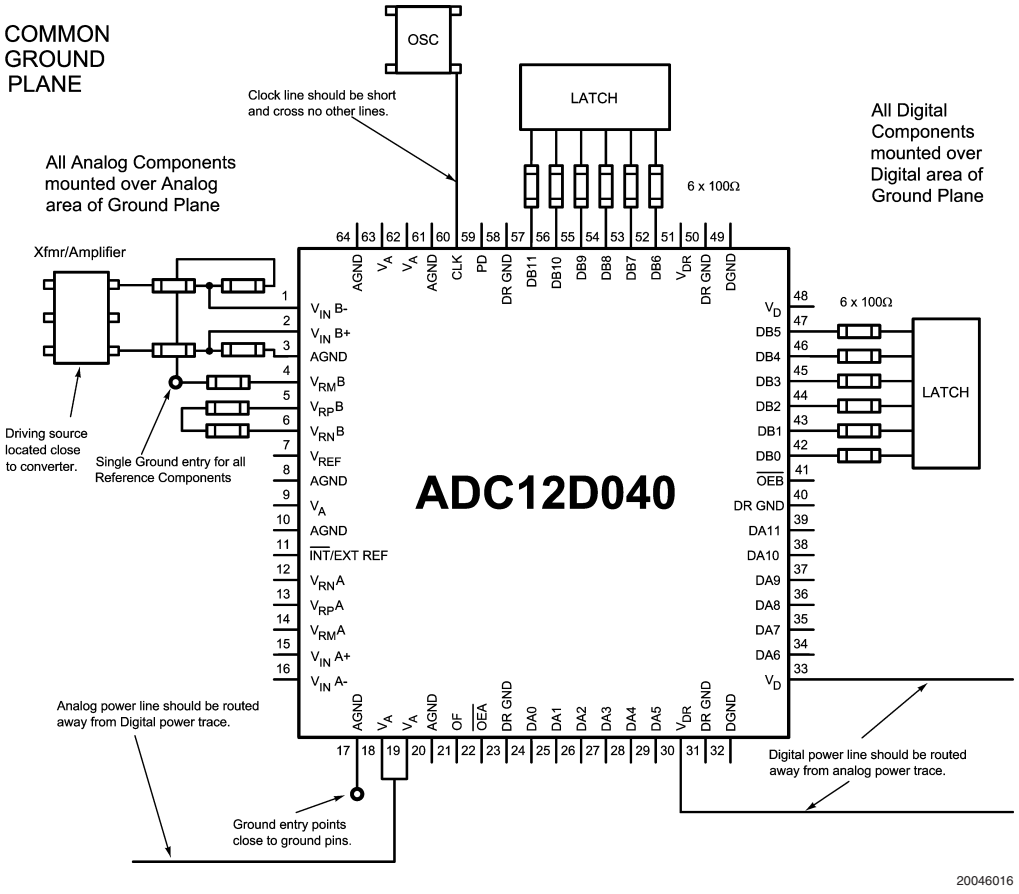


FIGURE 6. Example of a Suitable Layout

Applications Information (Continued)

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Generally, analog and digital lines should cross each other at 90˚ to avoid crosstalk. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. Even the generally accepted 90˚ crossing should be avoided with the clock line as even a little coupling can cause problems at high frequencies. This is because other lines can introduce jitter into the clock line, which can lead to degradation of SNR. Also, the high speed clock can introduce noise into the analog chain.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should *not* be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the analog ground plane.

Figure 6 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed in the analog area of the board. All digital circuitry and I/O lines should be placed in the digital area of the board. The ADC12DL040 should be between these two areas. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the analog ground plane at a single, quiet point. All ground connections should have a low inductance path to ground.

6.0 DYNAMIC PERFORMANCE

To achieve the best dynamic performance, the clock source driving the CLK input must be free of jitter. Isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in *Figure 7*. The gates used in the clock tree must be capable of operating at frequencies much higher than those used if added jitter is to be prevented.

Best performance will be obtained with a differential input drive, compared with a single-ended drive, as discussed in Sections 1.3.1 and 1.3.2.

As mentioned in Section 5.0, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal, which can lead to reduced SNR performance, and the clock can introduce noise into other lines. Even lines with 90˚ crossings have capacitive coupling, so try to avoid even these 90˚ crossings of the clock line.

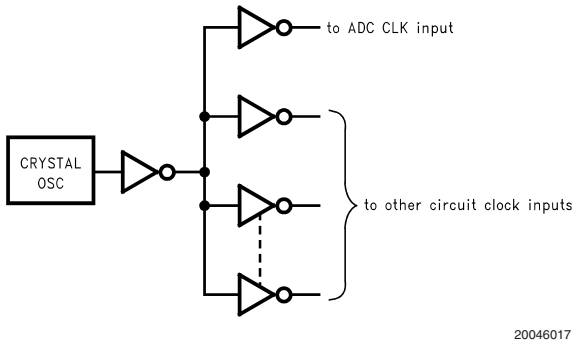


FIGURE 7. Isolating the ADC Clock from other Circuitry with a Clock Tree

7.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital components (e.g., 74F devices) to exhibit overshoot or undershoot that goes above the power supply or below ground. A resistor of about 47Ω to 100Ω in series with any offending digital input, close to the signal source, will eliminate the problem.

Do not allow input voltages to exceed the supply voltage, even on a transient basis. Not even during power up or power down.

Be careful not to overdrive the inputs of the ADC12D040 with a device that is powered from supplies outside the range of the ADC12D040 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_{DR} and DR GND. These large charging current spikes can couple into the analog circuitry, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital areas on the pc board will reduce this problem.

Additionally, bus capacitance beyond the specified 20 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could, again, be an apparent reduction in dynamic performance.

The digital data outputs should be buffered (with 74AC541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC12D040, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 100Ω.

Using an inadequate amplifier to drive the analog input. As explained in Section 1.3, the capacitance seen at the input alternates between 8 pF and 7 pF, depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. A small series resistor at each amplifier output and a capacitor across the analog inputs (as shown in *Figure 5*) will

Applications Information (Continued)

improve performance. The LMH6702 and the LMH6628 have been successfully used to drive the analog inputs of the ADC12D040.

Also, it is important that the signals at the two inputs have exactly the same amplitude and be exactly 180° out of phase with each other. Board layout, especially equality of the length of the two traces to the input pins, will affect the effective phase between these two signals. Remember that an operational amplifier operated in the non-inverting configuration will exhibit more time delay than will the same device operating in the inverting configuration.

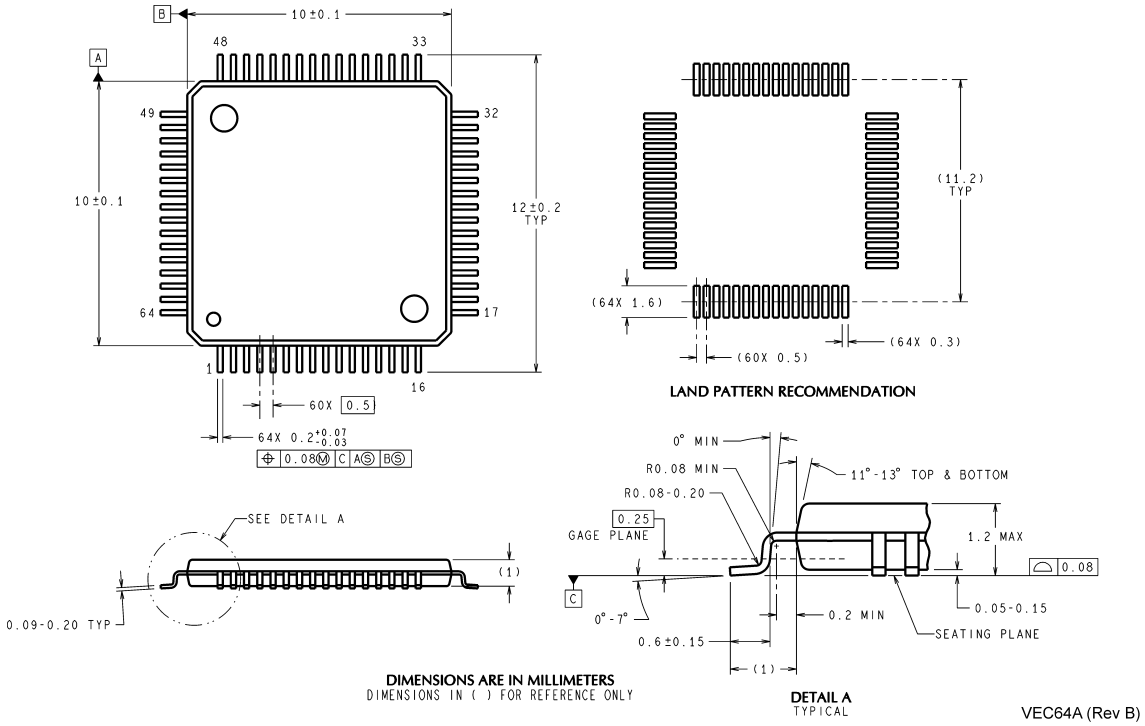
Operating with the reference pins outside of the specified range. As mentioned in Section 1.2, V_{REF} should be in the range of

$$1.0V \leq V_{REF} \leq 2.4V$$

Operating outside of these limits could lead to performance degradation.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR and SINAD performance.

Physical Dimensions inches (millimeters) unless otherwise noted



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